

CLAIMS

1. A method comprising:

generating a first encoded signal at an input to a dynamic bus in response to a transition at said input between a current clock cycle and a previous clock cycle; and

transmitting the first encoded signal on the bus.

2. The method of claim 1, further comprising

generating a second encoded signal at an input of a dynamic bus in response to no transition at the input between a current clock cycle and a previous clock cycle; and

transmitting the second encoded signal on the bus.

3. The method of claim 2, wherein the first encoded signal comprises a HIGH signal and the second encoded signal comprises a LOW signal.

4. The method of claim 1, wherein said generating the first encoded signal is performed independently of the actual values of a first data signal received at the input in the current clock cycle and a second data signal received at the input in the previous clock cycle.

5. The method of claim 1, further comprising receiving the first encoded signal at an output of the dynamic bus.

6. The method of claim 5, further comprising storing the encoded signal at the output.

7. The method of claim 6, further comprising comparing the first encoded signal received at the output in the current clock cycle to a second encoded signal received at the output in the previous clock cycle.

8. The method of claim 7, further comprising tracking the values of the signals received at the input in response to the encoded signals received at the output.

9. The method of claim 8, further comprising generating a first output signal at the output in the current clock cycle in response to the first encoded signal and the second encoded signal, said first output signal having a value identical to a value of a first input signal received at the input in the current clock cycle.

10. A dynamic bus comprising:
a bus line having an input node operative to receive a data signal and an output node;

a clock signal generator operative to generate a clock signal in a clock cycle;

an encoder coupled to the input node and the clock signal generator, said encoder operative to generate a first encoded signal in response to a transition at the input node between a current clock cycle and a previous clock cycle; and

a decoder circuit coupled to the output node and the clock signal generator.

11. The dynamic bus of claim 10, wherein the encoder comprises:

a storage device operative to store an input signal received at the input node of the encoder in a previous clock cycle;

a first domino gate coupled to the clock signal generator and including an input transistor having a gate coupled to the input node of the encoder;

a second domino gate coupled to the clock signal generator and including an input transistor having a gate coupled to the storage device;

an inverter including an input node and an output node coupled to the bus line;

an encoded signal node coupled to the input node of the inverter;

a first transistor coupled between the encoded signal node and a first discharge path through the input transistor in the first domino gate; and

a second transistor coupled between the encoded signal node and a second discharge path through the input transistor of the second domino gate.

12. The dynamic bus of claim 11, further comprising a second clock signal generator operative to generate a second clock signal having a timing approximately complementary to a timing of the clock signal generator,

wherein the storage device is coupled to and controlled by the second clock signal generator.

13. The dynamic bus of claim 12, wherein the storage device comprises:

a clocked flip flop having an output node and an input node coupled to the source of the input transistor of the first domino gate; and

an inverter coupled between the output node of the clocked flip flop and the gate of the input node in the second domino gate.

14. The dynamic bus of claim 11, wherein the decoder comprises circuitry operative to generate a decoded signal in response to an encoded signal received on the bus line.

15. The dynamic bus of claim 14, wherein the decoded signal comprises an output data signal having a value corresponding to the value of an input data signal received at the input node of the encoder in response to receiving an encoded signal from the bus line.

16. The dynamic bus of claim 14, wherein the decoder comprises a storage device having an input node and an output node, said storage device operative to store a decoded signal generated in a previous clock cycle.

17. The dynamic bus of claim 16 wherein the storage device comprises a clocked flip flop having a clock input coupled to the clock signal generator.

18. The dynamic bus of claim 16, wherein the decoder comprises:

a first PMOS transistor coupled between the input node of the storage device and the bus line, said first PMOS transistor having a gate coupled to the output node of the storage device;

a second PMOS transistor coupled between the input node of the storage device and the output node of the storage device, said first PMOS transistor having a gate coupled to the bus line;

a pair of stacked NMOS transistors coupled between the input node of the storage device and a discharge path, a first one of said pair of stacked NMOS transistors having a gate coupled to the bus line and a second one of said pair of stacked NMOS transistors having a gate coupled to the output node of the storage device;

an NMOS transistor having a gate and being coupled between the input node of the storage device and the bus line; and

an inverter coupled between the output node of the storage device and the gate of the NMOS transistor.

19. The dynamic bus of claim 11, further comprising a state machine operative to track the values of signal output from the decoder.